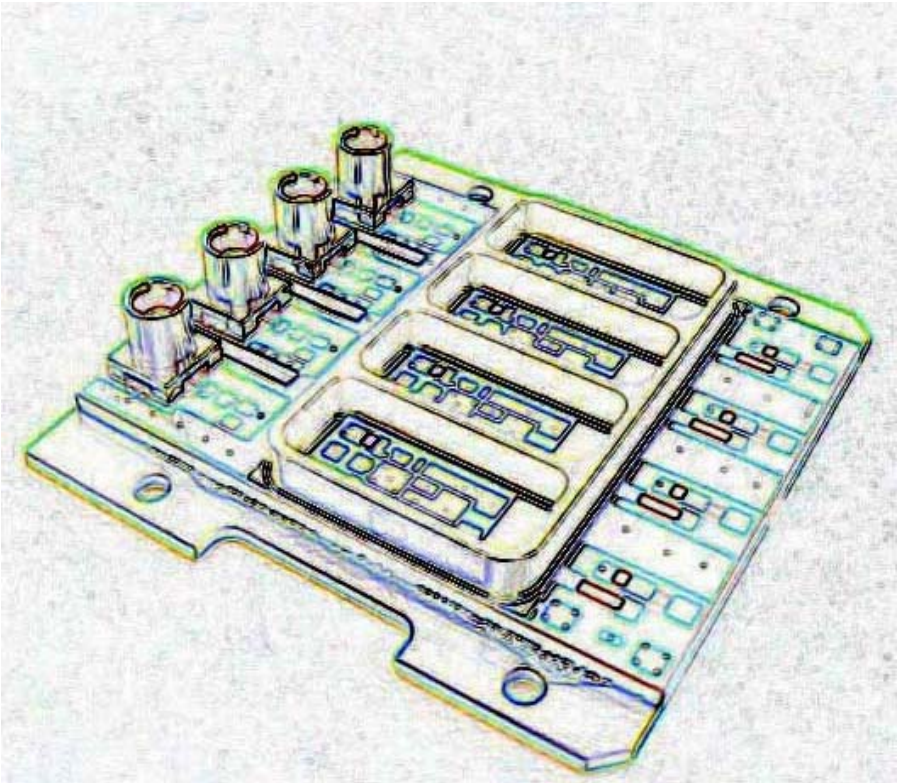
Low Temperature Co-Fired Ceramic Design Guidelines

DESIGN GUIDE



SEA CERAMIC TECHNOLOGIES
17755 Sky Park East, Suite CD
Irvine, CA 92614
714-540-5595

Revision: A

LTCC DESIGN GUIDELINES

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LTCC DESIGN GUIDELINES

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LTCC DESIGN GUIDELINES

SEA CERAMICS CAPABILITIES

MATERIAL SYSTEMS

- **DUPONT 951 TAPE SYSTEM**
  ALL GOLD
  MIXED SILVER/GOLD SYSTEM
  PT/AU - PD/AG - GOLD - SILVER - SURFACE METALIZATIONS
  ALL SILVER

- **FERRO A6M and A6S TAPE SYSTEMS**
  MIXED SILVER/GOLD SYSTEM
  ALL GOLD
  PT/AU - PD/AG - GOLD - SILVER - SURFACE METALLIZATIONS
  ALL SILVER

- HERAEUS "ZERO SHRINK" HERALOCK

- **SOLDER/EPOXY ATTACHMENT - RING FRAMES HEAT SINKS LEADS AND TIE BARS**

  LOW/HIGH TEMPERATURE SOLDER ALLOYS
  CU - MO - CU, CU-W, KOVAR, MOLYBDENUM AND AL-SI-C HEAT SINKS
  NICKEL/GOLD PLATED KOVAR / NI-FE SEAL RING, PINS AND LEADS
  COPPER LEADS AND PINS
  CERAMIC TIE BAR ATTACHMENT

- **SYSTEM TECHNOLOGY**

  LTCC DIGITAL / ANALOG/ MICROWAVE SUBSTRATES
  INTEGRAL MCM, RF AND OPTICAL PACKAGING
  BALL GRID ARRAYS
  PIN GRID ARRAYS (Strain reinforcement may be required).
  INTEGRATED PASSIVE COMPONENTS - RESISTORS, CAPACITORS, INDUCTORS AND FILTERS

- **SERVICES**

  LTCC
  THICK FILM
  CERAMIC MACHINING
  MCM DESIGN AND DATA CONVERSION
  SOLDER ASSEMBLY

LTCC DESIGN GUIDELINES

OVERVIEW

This document summarizes the design guides for use with Low Temperature Co-fired Ceramics (LTCC). This design guides define three levels of producibility as follows:

LOW VOLUME (POC / POD)

Substrates designed to Low volume (POC / POD) levels of producibility are fabricated in an environment that may push current state of the art LTCC process. Normal tolerances may have been exceeded, thus resulting in a higher risk situation where excessive touch up, rework and lower yields are incured and therefore have an impact on producibility, scheduling and cost. **A best effort fabrication requirement may be imposed on designs of this type.**

MEDIUM VOLUME

Substrates designed to these guidelines are capable of being produced with minimum inspection, touchup and rework resulting in reduced cost while maintaining acceptable circuit performance.

PRODUCTION

Product designed to these guidelines is fabricated in a semi-automated and manual production environment. These layout guides encourage larger geometry's and wider tolerances to reduce inspection and eliminate rework. The overall goal is to produce product at the lowest possible price while maintaining aggressive shipment schedules.

Minimum and preferred dimensions

Minimum and preferred dimensions have been provided whenever possible. If preferred dimensions are provided they should be considered the optimum for the process. When a preferred condition is not provided, the condition defined should be considered a minimum. Good design practice calls for use of minimums only in circumstances where circuit performance and fit cannot tolerate more liberal preferred limits. **Use of minimums should be avoided whenever possible.**

Physical Considerations

The minimum thickness for any portion of a LTCC substrate .0222", with approval. Any design using a LTCC substrate should allow for a ± .5% shrinkage variable.

The minimum standard camber allowed is .002"/in/in. Product requiring less camber may be quoted at increased cost.

The following pages of this design provides a detailed description of allowable shapes, dimensions and spacing for designing LTCC substrates and packages.

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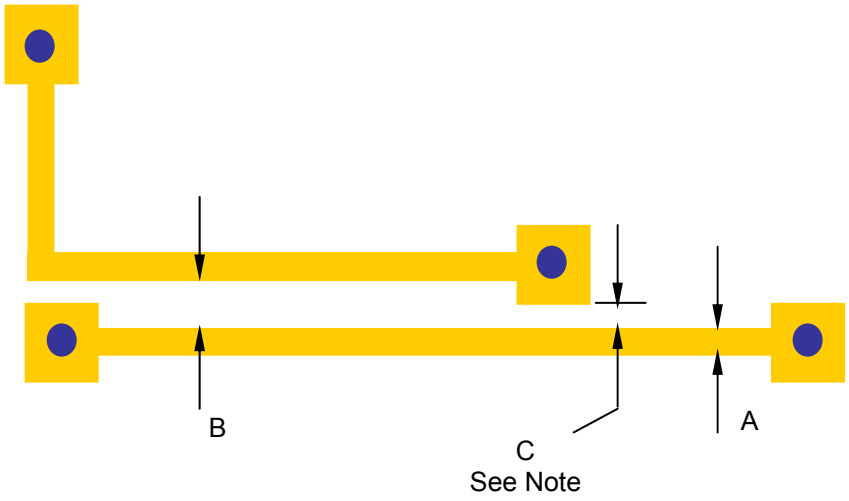
LTCC DESIGN GUIDELINES

CONDUCTORS

Conductor line width and spacing.



	PREFERRED DIMENSIONS			MINIMUM DIMENSIONS		
LTCC CLASS	**A**	**B**	**C**	**A**	**B**	**C**
POD/POC	5 mils	7 mils	5 mils	3 mils*	4 mils*	3 mils*
Medium Volume	6	8	6	4	5	4
Production	10	10	10	8	8	8

*** Must be approved by Sea Ceramics technical staff for each submitted design prior to acceptance.**

NOTE: Normal design practice uses a standard grid spacing where the sum of the line width and space equal the pitch. If an LTCC "Medium Volume" design class is constructed on a 16 mil pitch (8 mil lines and spaces), catch pads overlaps will cause spacing violations. These spacing violations are acceptable for short distances but causes higher probability of added inspection and touch up. This condition causes increased costs and possible schedule impact. **A larger pitch is recommended whenever possible**.

Where design density is at a maximum and catch pads pose a potential shorting problem, conductor lines may be terminated directly to the via without a catch pad. Please contact Sea Ceramics technical staff for specific applications.

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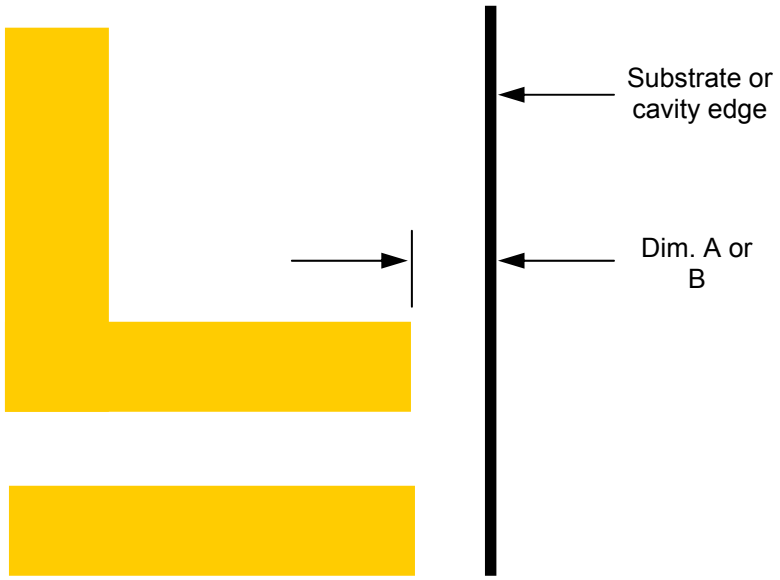
LTCC DESIGN GUIDELINES

CONDUCTORS

Conductor to edge of substrate/cavity clearance.



	PREFERRED DIMENSIONS			MINIMUM DIMENSIONS		
LTCC CLASS	**A SURFACE**	**B BURIED**	**RF GROUNDS***	**A SURFACE**	**B BURIED**	**RF GROUNDS***
POD/ POC	10 mils	10 mils	10 mils	5 mils*	5 mils*	To edge*
Medium Volume	10 mils	10 mils	10 mils	5 mils*	5 mils*	5 mils*
Production	15 mils	15 mils	15 mils	10 mils	10 mils	10 mils

*Conductors and ground/power planes designed less than 5-10 mils to the substrates/cavity edge can result in edge exposure or smearing resulting in possible **shorting** during substrate mounting. Also, there may be some **"sloping or rounding"** of the last 5 - mils of the conductor near cavity edges (this includes substrate edges defined by a cavity). Please verify that this condition will not pose electrical design or processing issues prior to completing lay out.

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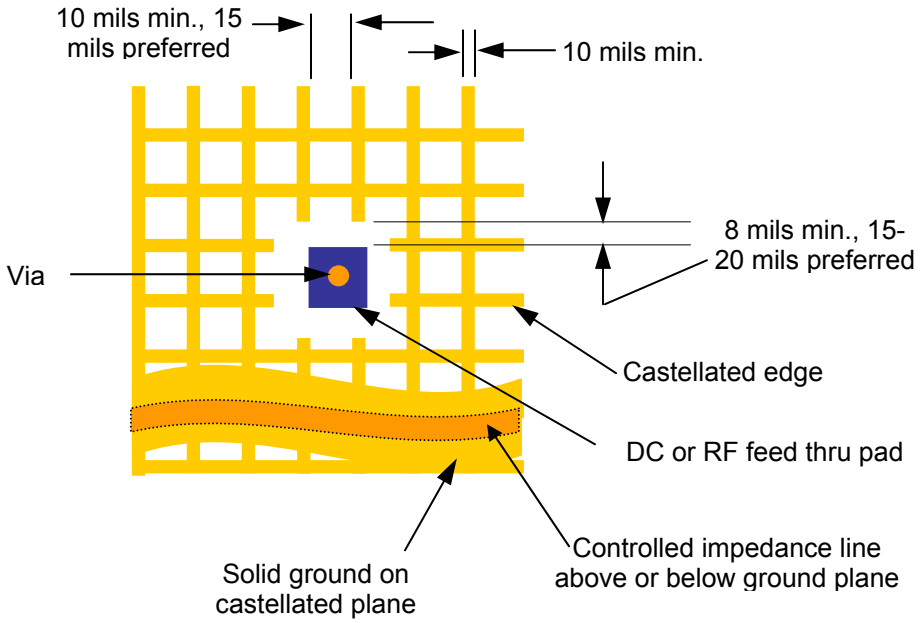
LTCC DESIGN GUIDELINES

GROUND AND POWER PLANES

Large exposed conductor areas such as planes may be solid. Buried planes should be gridded where ever possible. A typical gridded plane will have 10 mil lines with 15-20 mil openings* (see below). Areas on the ground plane may be solid to provide shielding to transmission lines and other critical signals when required. The edges (around substrate perimeter and cavities) of all ground planes must be castellated to promote proper lamination adhesion between tape layers (Sea Ceramics recommends at least 50% open area). Feed through vias/pads on buried plane layers should have a 15-20 mil isolation clearance between the feed through and the plane (8 mils absolute min. upon design review). The grid pattern of planes on adjacent layers should be offset wherever possible to provide a uniform top and bottom substrate surface.



* 10 mil lines with 10 mil openings minimum. Ground plane grids should be maximized when ever possible to improve yield and reduce cost.

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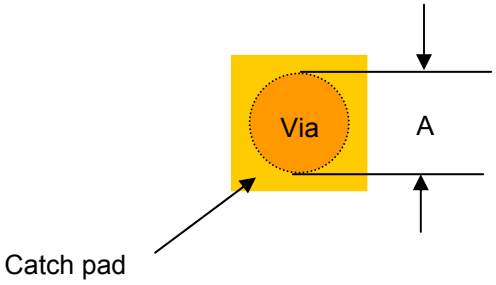
LTCC DESIGN GUIDELINES

ELECTRICAL VIAS

Electrical via sizes for standard tape thicknesses (see table below). A maximum of three via diameters on any tape is offered as standard processing. Other via sizes and quantities per layer is available upon request.



		PREFERRED DIMENSIONS			MINIMUM DIMENSIONS		
LTCC CLASS	**Tape Thickness ***	**3.7 mil**	**5.2 mil**	**7.4 - 8.2 mil**	**3.7 mil**	**5.2 mil**	**7.4 - 8.2 mil**
POD/ POC	**Via dia. A****	8,10 mils	8,10 mils	8,10 mils	4 mils	6 mils	6 mils
Medium Volume	**Via dia. A****	8,10 mils	8,10 mils	8,10 mils	4 mils	6 mils	6 mils
Production	**Via. dia. A****	8,10 mils	8,10 mils	8,10 mils	6 mils	6 mils	8 mils

* Approximate fired thickness.
** As punched unfired diameter (Apply specific shrinkage factor to determine fired diameter).

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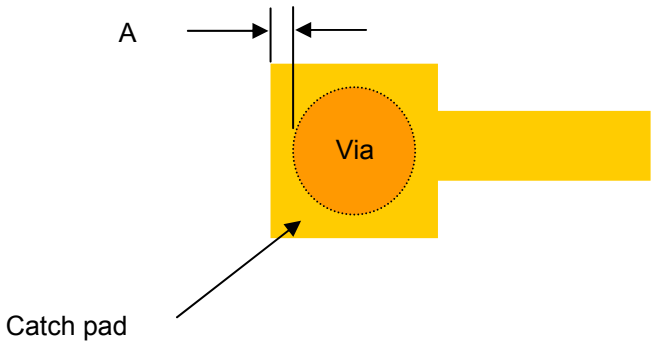
LTCC DESIGN GUIDELINES

ELECTRICAL VIAS

Catch Pads

Catch pads above and below each via shall overlap the via on all sides by the specified distance (see table below). Exceptions are areas of dense routing that do not permit the use of catch pads over vias (conductor lines are then terminated directly to vias*).

Catch pads may be excluded from RF transition vias.



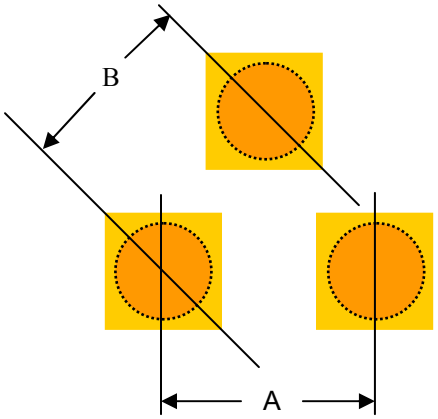
LTCC CLASS	A (min.)
POD/ POC	1 mil
Medium Volume	2 mils
Production	4 mils

* This design practice is not encouraged except where absolutely necessary as it may affect electrical yields.

LTCC DESIGN GUIDELINES

ELECTRICAL VIAS

Electrical via to via spacing on the same layer



LTCC CLASS	A (min.)	B (min.)
POD/ POC	2.5 x Via size	2.5 x Via size
Medium Volume	3 x Via size	3 x Via size
Production	3 x Via size	3 x Via size

NOTE: Thermal and RF vias are excluded from this criteria.

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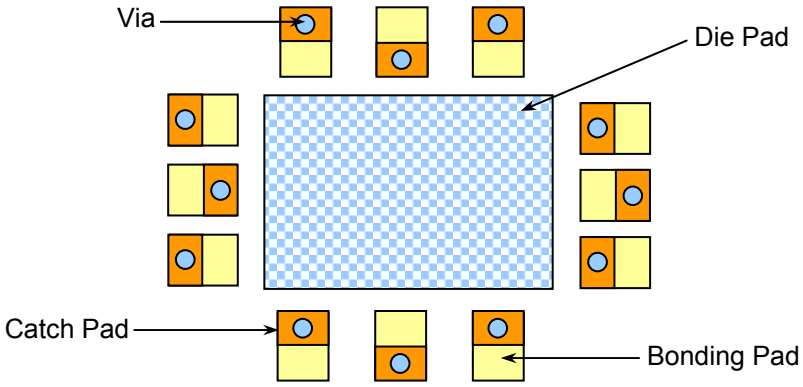
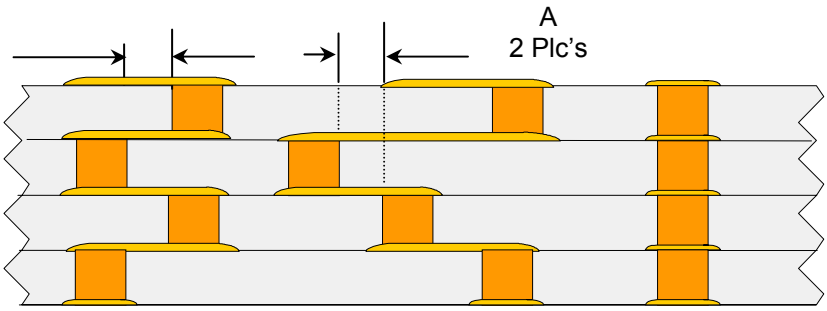
LTCC DESIGN GUIDELINES

ELECTRICAL VIAS
Where design density necessitates long strings of vias, the vias should be staggered to prevent snapstrate type cracking. The diagram below is an example of a staggered via pattern.



Electrical via to electrical via stagger for layer to layer connections. Vias may stagger (zigzag) vertically to minimize blockage of routing channels and reduce via "posting" effects. The diagram below is an example of acceptable via staggering techniques.

LTCC CLASS	A (min.)
POD/ POC	Tangent
Medium Volume	1 Via diameter
Production	1 Via diameter



Acceptable zigzag Pattern | Preferred Staircase pattern | Stacked vias

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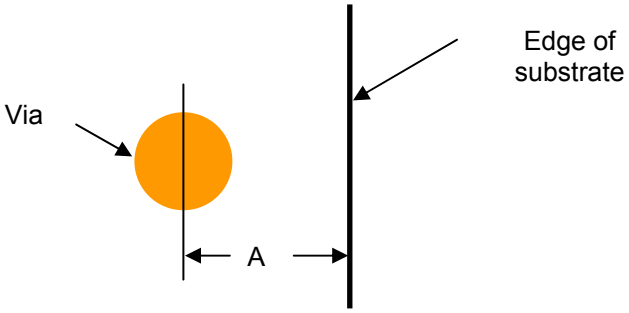
LTCC DESIGN GUIDELINES

ELECTRICAL VIAS

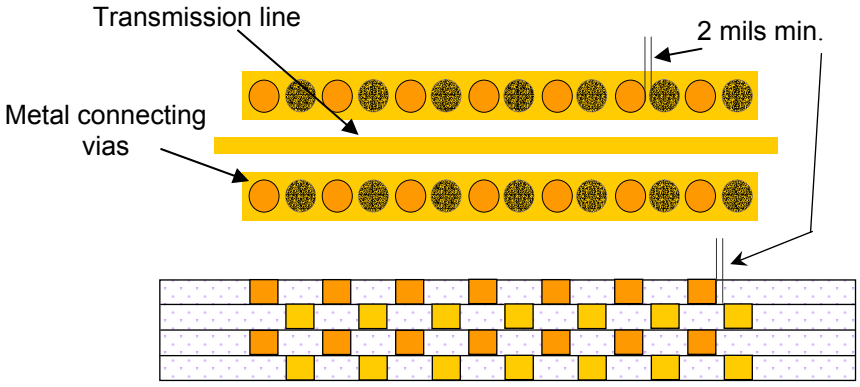
Electrical via to edge of substrate.



LTCC CLASS	A (min.)
POD/ POC	3 Via diameters (18 mils minimum)
Medium Volume	4 Via diameters (25 mils minimum)
Production	4 Via diameters (25 mils minimum)

RF VIAS

Designs requiring high frequency lines and controlled impedance lines may require buried coaxial type shielding which is accomplished by placing vias parallel to the controlled lines through out the shielded cross sectional area. RF vias may be placed as close as 2 mils apart (horizontal displacement on adjacent layers) as long as they are electrically common to each other. RF vias may also be stacked if required as long as they maintain 2 via diameters pitch minimum **(Stacked vias may not be hermetic**). See diagram below. Also see page 14.



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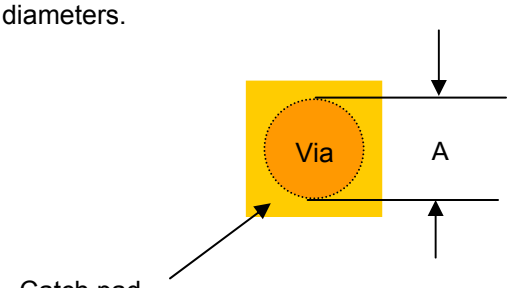
LTCC DESIGN GUIDELINES

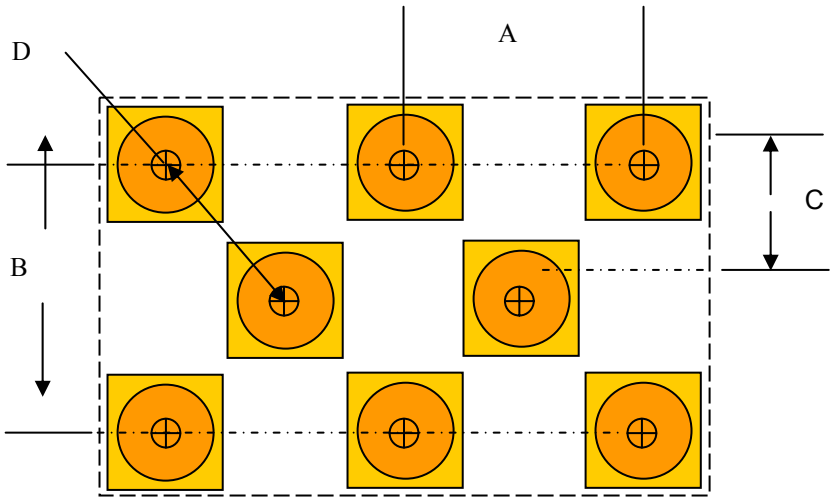
THERMAL VIAS

Available thermal vias diameters.



LTCC CLASS	A Dia. (min.)
POD/ POC	4, 6, 8,10 mils
Medium Volume	4, 6, 8,10 mils
HV Production	6, 8,10 mils

Thermal via pattern



Thermal via array dimensions

Via Diameter (Mils)	A	B	C	D
4	9	9	4.5	6.36
6	13.5	13.5	6.75	9.55
8	18	18	9	12.73
10	22.5	22.5	11.25	15.9
12	30	30	15	21.21
15	45	45	22.5	31.82

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LTCC DESIGN GUIDELINES

THERMAL VIAS

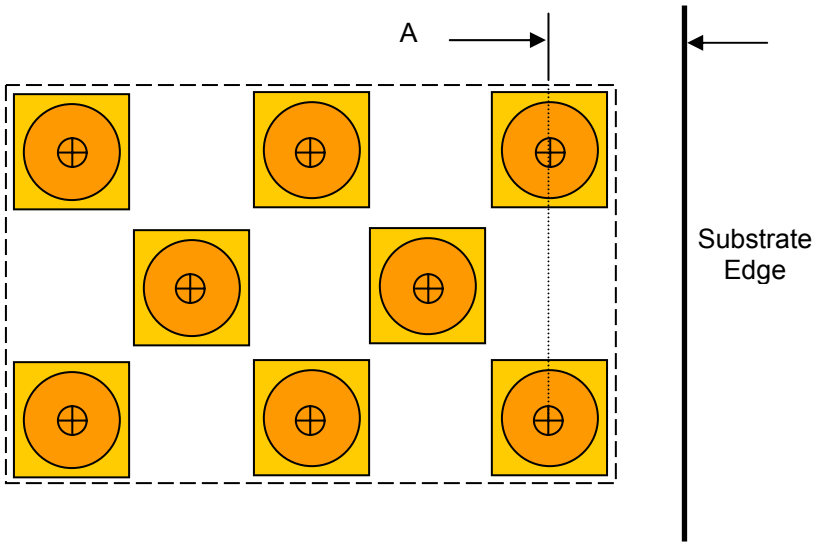
The maximum thermal via array size is 250 mil, length or width. Larger thermal arrays using larger via diameters with 3 x via diameter spacing are available upon request. While the thermal vias shown in this design guide show individual cover pads a solid metal single pad covering all vias is acceptable. This approach helps spread heat reducing thermal impedance.

To best reduce thermal impedance, select a via diameter that will allow for maximum packing density under the component dissipating the heat. Also try and center a via directly under a known thermal junction in the component.

Stacked thermal vias are the most efficient method of reducing thermal impedance. Please keep in mind that stacked thermal via arrays **may not be hermetic** to helium leak testing.

Additional thermal performance and design information is available in our LTCC Design CD.

Thermal via to edge of substrate clearance.



LTCC CLASS	A Minimum	A Preferred
POD/ POC	60 mils	100 mils
Medium Volume	60 mils	150 mils
Production	150 mils	150 mils

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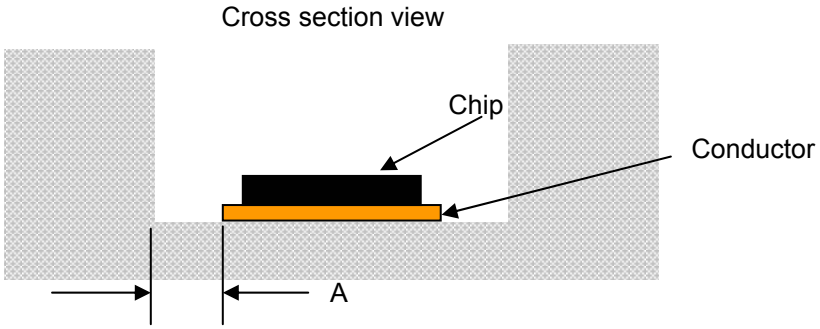
LTCC DESIGN GUIDELINES

CAVITIES

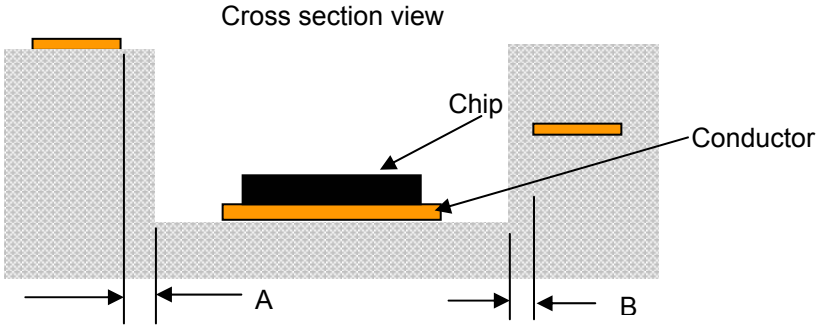
Cavity bottom conductor to cavity wall clearance.



LTCC CLASS	A Minimum *
POD/ POC	2.5 mils
Medium Volume	5 mils
Production	10 mils

* Bottom conductor electrical connection can be made through cavity wall, if required, but should not exceed 25% of the wall length, 50% maximum. Castellated metallization designs may be used to meet this requirement.

Exposed/buried conductor to cavity wall clearance.



LTCC CLASS	A Exposed	B Buried
POD/ POC	5 mils	10 mils
Medium Volume	5 mils	10 mils
Production	15 mils	15 mils

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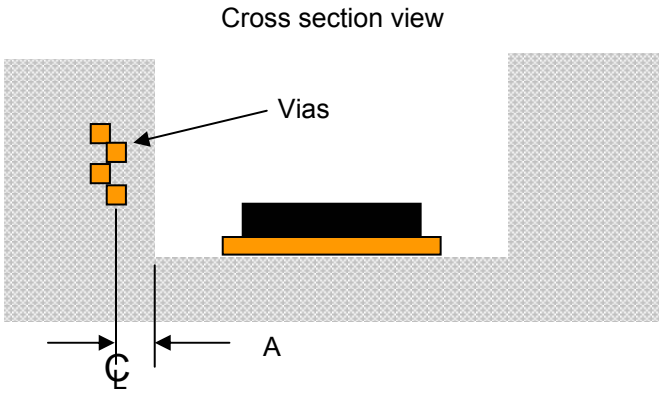
LTCC DESIGN GUIDELINES

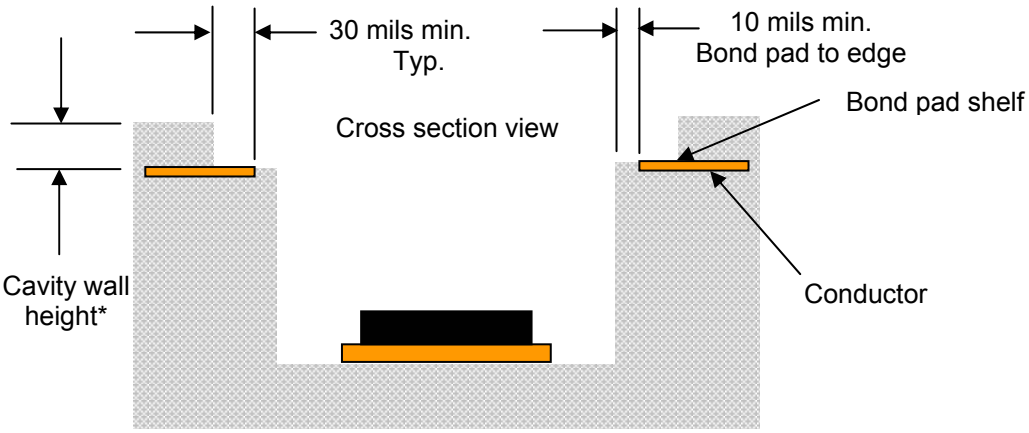
CAVITIES

Via to cavity wall clearance.



LTCC CLASS	A
POD/ POC	2.5 x via Size
Medium Volume	2.5 x via Size
Production	2.5 x via Size

Bond Shelf



Note: Cavity wall height above bond shelf shall be reviewed prior to design acceptance.

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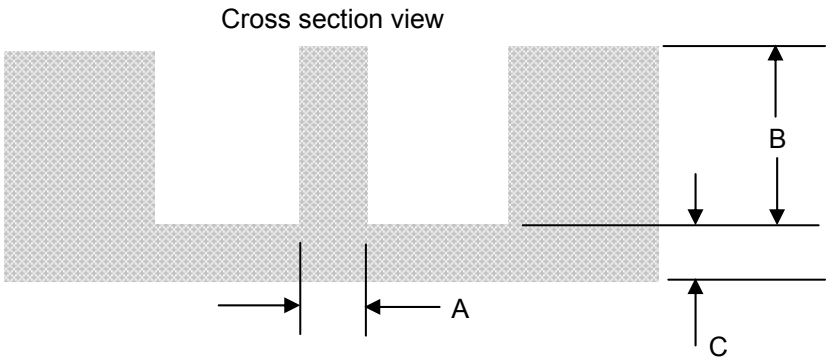
LTCC DESIGN GUIDELINES

CAVITIES

Cavity to cavity spacing



MINIMUM DIMENSIONS

LTCC CLASS	A - Wall width	B - Cav depth	C - Base thickness
POD/ POC	50 mils	2 x "A" dim.	22.2 mils minimum*
Medium Volume	50 mils	2 x "A" dim.	22.2 mils minimum*
Production	50 mils	2 x "A" dim.	22.2 mils minimum*

NOTES:

1. As fired cavity walls shall not exceed 500 mils in length.

2. Post fired machined cavity walls shall not exceed 2 inches in length.

3. Minimum cavity depth is one tape layer. Bond shelves are considered cavities.

* Requires review

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LTCC DESIGN GUIDELINES

SPECIAL HIGH FREQUENCY DESIGN PROVISIONS AND SUPPORT

AVAILABLE DIELECTRIC K's
Available tape dielectric constants of 5.9 ± .15 (Ferro low loss), 7.8 (Dupont 951), 9.1 Heraeus (CT2000) and 7.3 (Heraeus Heralock)

DIMENSIONAL TOLERANCES
Dielectric Z thickness tolerance is ± .0002" / layer after firing (4.5 – 5 mil green tape). Thicker 10 mil tapes may exhibit up to ± .0003" / layer shrinkage variability. **The minimum allowable substrate thickness in any portion of the design is 22.2 mils.** Design thickness' less than 25 mils require review. The thinner cross section areas of the design may exhibit more camber/warping than thicker areas.

Via and cavity positional tolerance is ± .3% after firing.

Layer to layer alignment is ± .001".

Cavity X,Y tolerance is ± .005" / side.

Critical line width and space tolerance is ± .0005", minimum.

Buried resistor tolerance is 30% dependent upon design. Contact Sea Ceramics for specific details. Tighter tolerances may be attempted under a best effort condition.

VIAS AND CATCH PADS
Vias may be stacked in any manner for RF transition and grounding applications. Stacked vias running straight through the complete substrate cross section **may not be hermetic**.
Catch pads over vias are preferred where possible but may be omitted where electrical performance would be compromised.

GROUND PLANES
Internal ground plane metallization should be gridded wherever possible. Ground planes may be made solid in the areas above, below, and adjacent to critical transmission lines (See page 3).
Minimum grid pattern is .01"lines with .01" openings. A 33%-50% opening to line ratio is preferred wherever possible. The minimum isolation distance between an electrical feed through via/pad and the ground plane is .008".

PRECISION LINE WIDTH PROCESS CONTROL AND INSPECTION
Sea Ceramics will perform special measurements of critical lines and spaces when notified prior to layout and fabrication of the substrate. The design database, mylar artwork and green fire dimensions will be closely monitored to ensure compliance to design. Critical dimensions should be recorded in a table similar to that shown in Appendix B. This table should be accompanied with a picture or diagram of the referenced measurement points.

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LTCC DESIGN GUIDELINES

RESISTORS

Resistors may be designed using the following sheet resistivity values:

SURFACE RESISTORS

SHEET RESISTIVITY VALUES

Material System	13Ω/□	100Ω/□	1,000Ω/□	10,000Ω/□	100,000Ω/□
Dupont 951	YES	YES	YES	YES	YES
Ferro A6-S	YES	YES	YES	YES	YES
Ferro A6-M	YES	YES	YES	YES	YES

BURIED RESISTORS

SHEET RESISTIVITY VALUES

Material System	35Ω/□	100Ω/□	1,000Ω/□	10,000Ω/□	100,000Ω/□
Dupont 951	YES	YES	YES*	YES*	NO
Ferro A6-S	YES	YES	YES*	YES*	NO
Ferro A6-M	YES	YES	YES*	YES*	NO

* 1K/Sq. and higher resistor sheet values may exhibit greater variation to tolerance.

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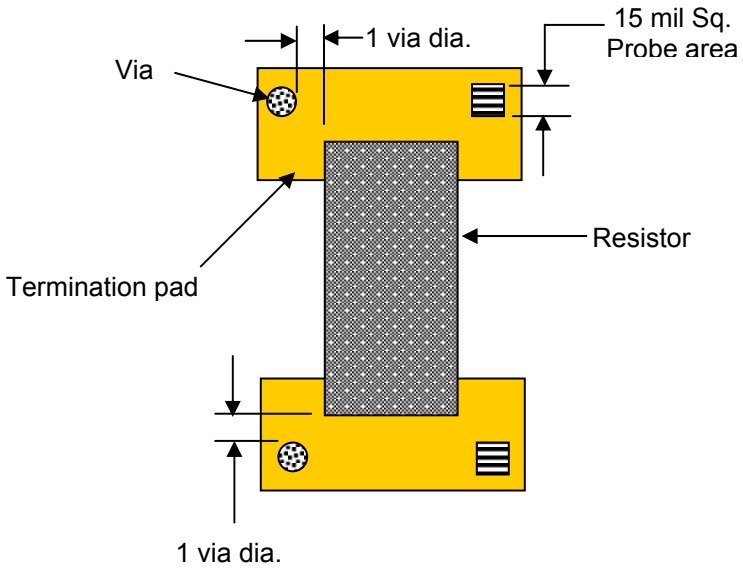
LTCC DESIGN GUIDELINES

RESISTORS

All resistors that are to be measured or trimmed to value should have, as a minimum, a 10 mil x 10 mil (15 mil preferred) probe area free of resistor material or overcoat material. In addition, as a minimum, terminating vias must be 1 via diameter away from the resistor or cover coat materials. Trimmed to value tolerances should be discussed with Sea Ceramics technical personnel prior to "locking" in designs. Resistors designed in parallel should be avoided**. Any design using parallel resistors networks must be identified and approved during design review.** Sea Ceramics cannot take responsibility for product losses resulting in un-identified parallel resistor networks.

The minimum tolerance for "as fired" surface or buried resistors is ± 30%.



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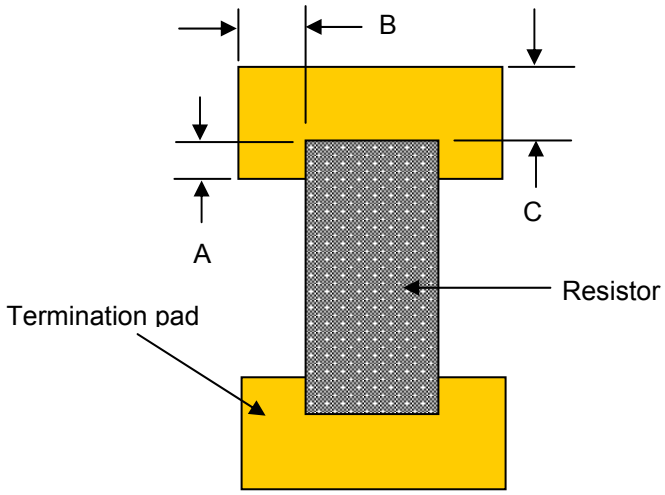
LTCC DESIGN GUIDELINES

RESISTORS

Resistor to conductor termination overlaps for surface and buried resistors.



LTCC CLASS	A Min.	B Min.	C Min.	A Preferred	B Preferred	C Preferred
POD/ POC	5 mils*	5 mils*	5 mils*	10 mils	10 mils	10 mils
Medium Volume	10 mils	10 mils	10 mils	>10 mils	>10 mils	>10 mils
Production	10 mils	10 mils	10 mils	>15 mils	>15 mils	>15 mils

***NOTE: The resistor design criteria noted above does not include metallization area required to probe resistors during measurement or laser trimming. Five-mil criteria may affect resistor stability, cost and schedule.**

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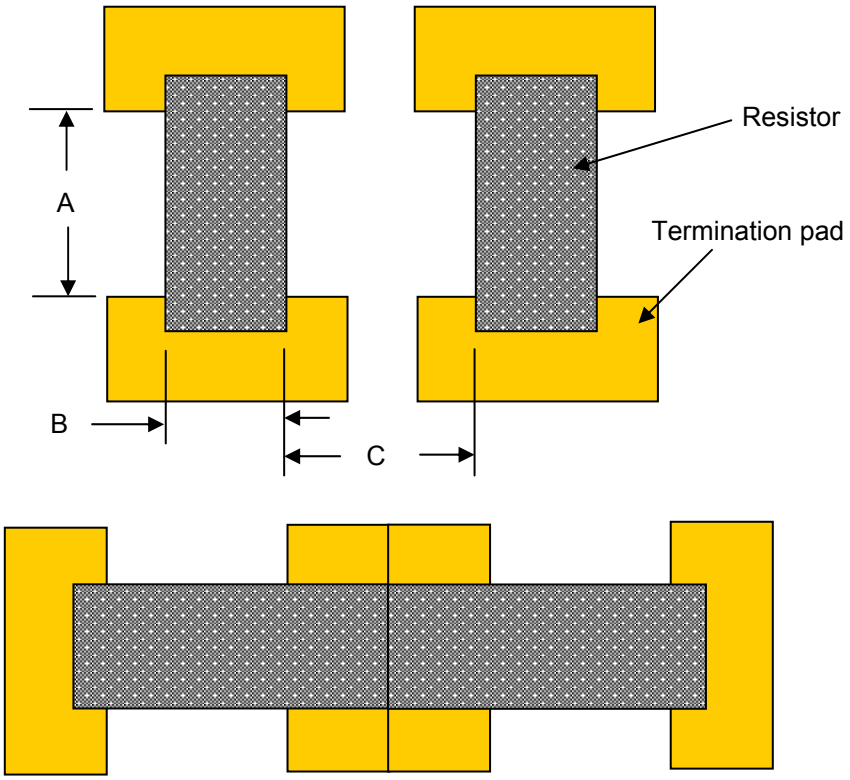
LTCC DESIGN GUIDELINES

RESISTORS

The minimum resistor length (between conductors) and width.

The maximum buried resistor size is 70 mils x 70 mils. Buried resistor coverage shall not exceed 15%. The maximum number of sheet resistivities per buried layer is two; maximum number of surface sheet resistivities is three.
Resistor to resistor spacing for resistors of the same sheet resistivity on the same layer. Resistors of the same sheet value with a common termination pad may abut.



Abutting Resistors

LTCC CLASS	A Min.	B Min.	C Min.	A Preferred	B Preferred	C Preferred
POD/ POC/RF	15 mils	15 mils	30 mils	40 mils	40 mils	>50 mils
Medium Volume	20 mils	20 mils	40 mils	40 mils	40 mils	>50 mils
Production	30 mils	30 mils	50 mils	40 mils	40 mils	100 mils

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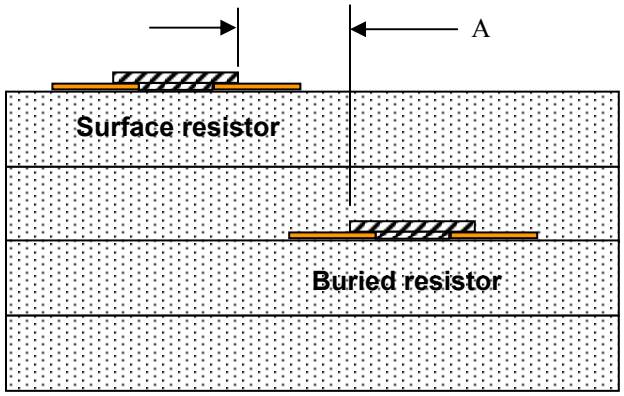
LTCC DESIGN GUIDELINES

RESISTORS

Spacing for surface to buried resistors or buried resistors on different tape layers.



Cross section

LTCC CLASS	A Min.	A Preferred
POD/ POC	50 mils	>50 mils
Medium Volume	50 mils	>50 mils
Production	50 mils	200 mils

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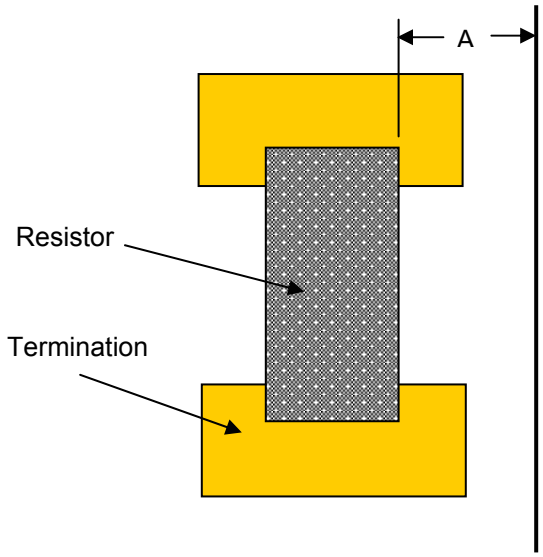
LTCC DESIGN GUIDELINES

RESISTORS

Resistor to edge of substrate clearance.



	SURFACE	BURIED
LTCC CLASS	**A Min.**	**A Min.**
POD/ POC	25 mils	>50 mils
Medium Volume	25 mils	>50 mils
Production	25 mils	200 mils

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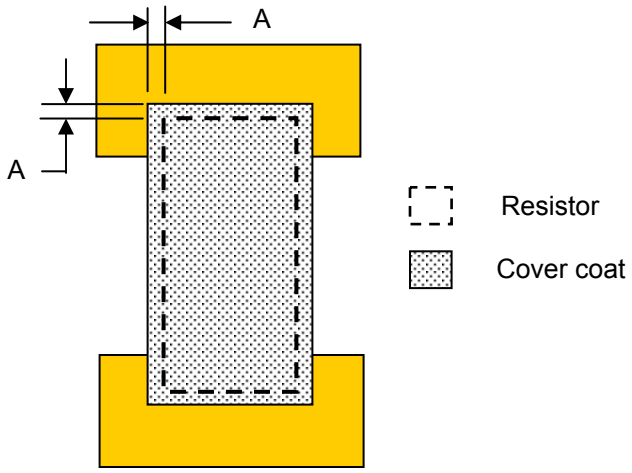
LTCC DESIGN GUIDELINES

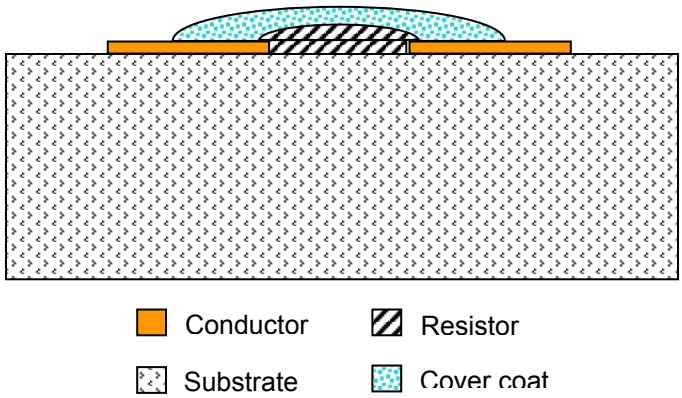
RESISTORS

Resistor cover coat overlap.

TOP View



Cross Section View



LTCC CLASS	A Min.
POD/ POC	5 mils
Medium Volume	10 mils
Production	10 mils

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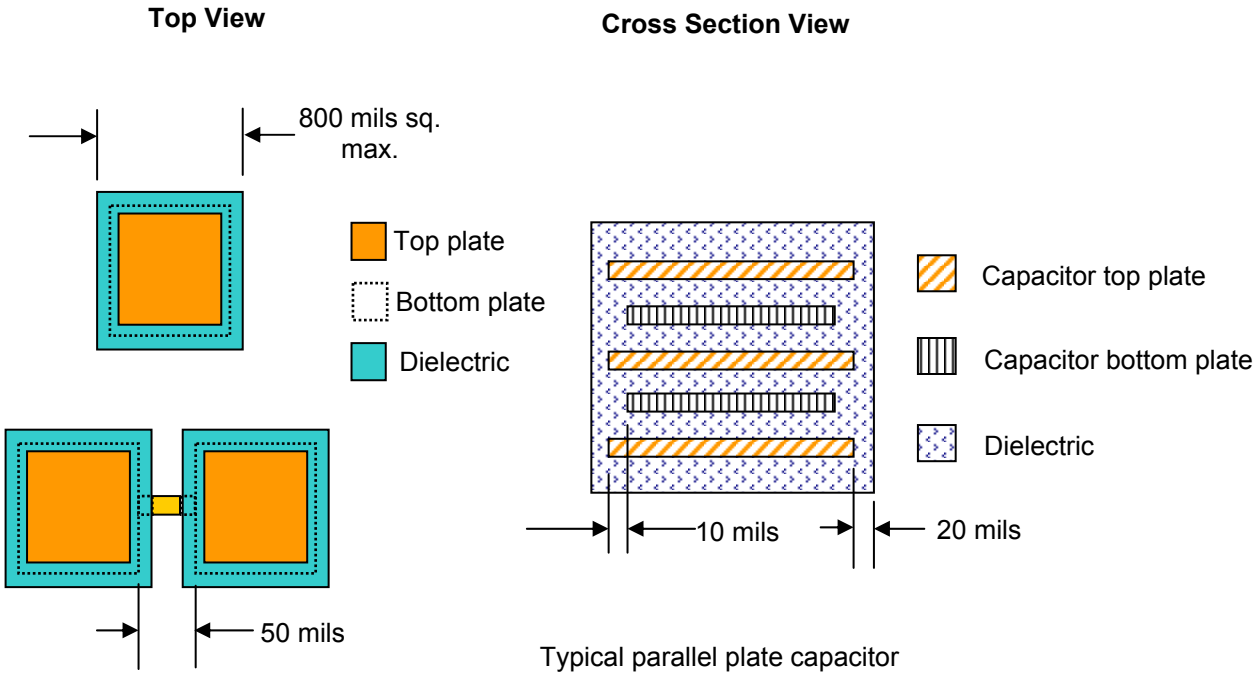
LTCC DESIGN GUIDELINES

CAPACITORS

Capacitors may be fabricated by placing parallel plates on adjacent tape layers. Capacitance values up to 450 pico farrads/ in^2 may be fabricated using standard Dupont K 7.8 tapes or 350 pico farrads/ in^2. for Ferro K 5.9 A6 tape. Higher capacitance values up to 45,000 pico farrads/ in^2 have been demonstrated by using K100 – K300 dielectrics.

The largest buried capacitor plate on standard LTCC tapes allowed is 800 mils square, but in no case shall exceed 50% of the substrate cross sectional area. The maximum plate size allowed when using K100-300 dielectrics is .28" sq. (or equivalent area, see page 22). A minimum .040" substrate cross section applies when using K100-300 dielectrics. When using high K dielectrics, symmetry is important. Design the high K capacitor towards the center of the substrates cross section. Off center design may result in ceramic warping during firing. Breakup capacitor plates when higher values are required, and if necessary the use of multiple tape layers is acceptable. Capacitor plates on alternate layers should overlap by 10 mils minimum on each side to eliminate registration errors that would affect electrical performance.

Please contact Sea Ceramics technical staff for specific applications and new developments.



Typical parallel plate capacitor

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LTCC DESIGN GUIDELINES

TYPICAL CAPACITOR DIELECTRIC SYSTEMS*

	Ferro		Dupont	
	High K	**LTCC**	**High K**	**LTCC**
Dielectric Type	X7R	NPO	X7R	NPO
Dielectric K	200	5.8-6	300	7-8
Cap Range (pf)**	20-2300	1-100	30-3400	1-200
Largest Pad size allowed - in^2 (mm^2)	.076(49)	.303(198)	.076(49)	.303(198)
Dissipation Factor (%DF)	<2.0%	<0.3%	<2.0%	<0.3%
Insulation Res. @ 100VDC	$>10^{11}$ ohms	$>10^{12}$ ohms	$>10^{11}$ ohms	$>10^{12}$ ohms
Breakdown voltage (min.)	>200 VDC	>500 VDC	>200 VDC	>500 VDC
Capacitance tolerance	± 20%	± 20%	± 20%	± 10%
Cap. Pad Metallization	Silver/ Gold*	Silver/ Gold*	Silver/ Gold*	Silver/ Gold*

* Please check for availability
** Using silver conductors - .025”x.025” minimum plate size
1. Gold typically generates 20 - 30% less capacitance than silver
2. Typical dielectric fired thickness is .0015”

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LTCC DESIGN GUIDELINES

INDUCTORS

Spiral and helix style inductors are available in surface or buried form. These inductors may be combined with capacitors and resistors to form RC or LRC circuits. Buried thick print silver (100µ max.) inductor spirals are available on a developmental best effort basis. **Electrical performance cannot be guaranteed and the use of pre-design test coupons is encouraged prior to finalizing product design**

Inductors may be designed 3 dimensionally (x, y, z) for optimum electrical performance.

Please contact Sea Ceramics technical staff for specific applications.

POST FIRED CONDUCTORS

Available metallization.

Sea Ceramics offers many surface metallization on LTCC to meet your particular design requirements.

SILVER	**GOLD**	**AL WIRE BONDABLE GOLD**	**PT/AU**
PD/AG	**PT/PD/AG**	**SOLDERABLE AG**	**SOLDERABLE AU**

NI/AU PLATE*

* In development

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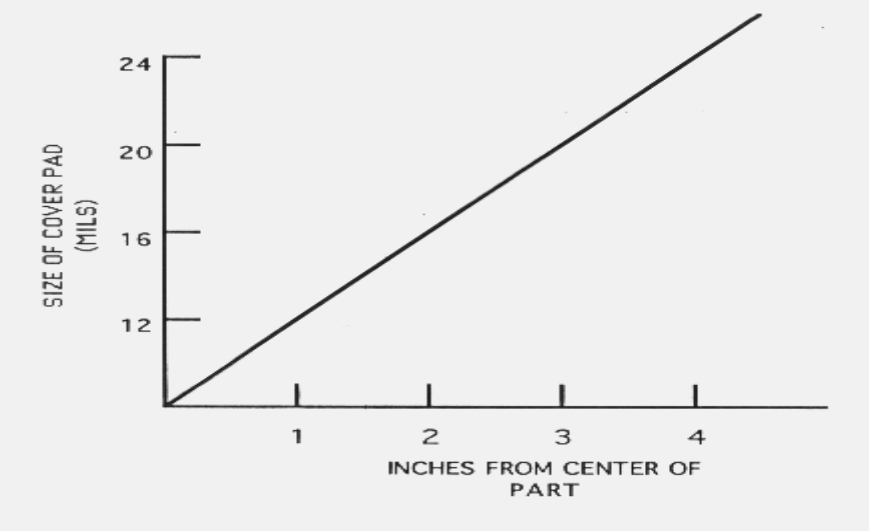
LTCC DESIGN GUIDELINES

POST FIRED CONDUCTORS

Cover pad design considerations when post print and firing surface metallization over LTCC vias.

LTCC products have, on an average, about a .3% variability in shrinkage during firing. If post printed catch pads are designed to small there is a probability that the catch pad and via would not line up (overlap) during printing, resulting in an electrical open. Please see the following two diagrams for recommended cover pad dimensions when designing surface metallization routing.

COVER PAD DIMENSION VS. DISTANCE FROM CENTER OF SUBSTRATE*



POSSIBLE VIA LOCATION VS. DISTANCE FROM CENTER OF SUBSTRATE*

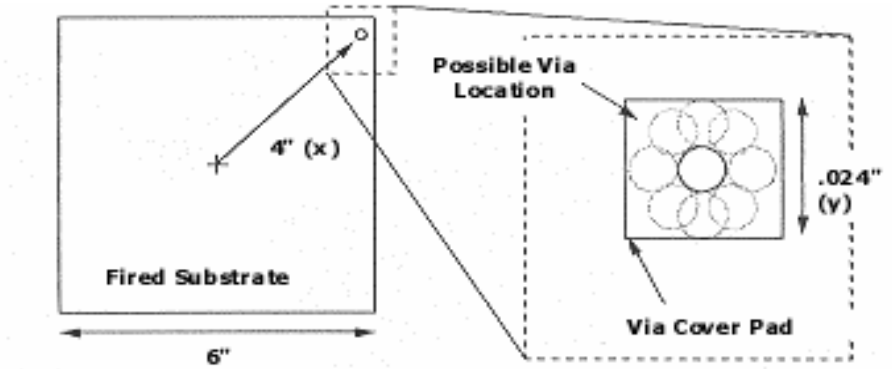


Figure 7: Via Cover Pad Example

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LTCC DESIGN GUIDELINES

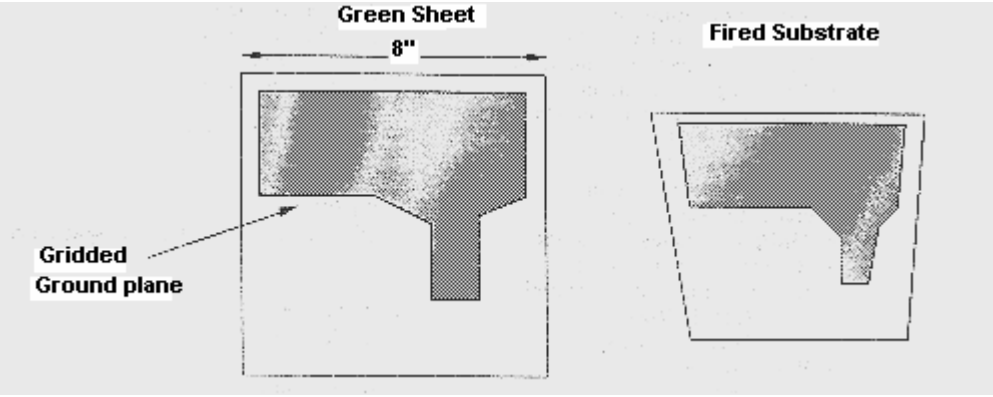
POST FIRED CONDUCTORS

Metal distribution and its effect on LTCC shrinkage.

Uneven metal distribution can cause distortion of the LTCC dielectric during firing. This is caused by a slight mis-match in shrinkage between the dielectric and the metallization during firing. When designing large conductors or ground planes proper even distribution of metallization is important to the uniformity of the finished LTCC substrate.

The following diagram shows an exaggerated view of LTCC distortion due to uneven metal distribution,

LTCC DISTORTION DUE TO UNEVEN METAL DISTRIBUTION*



* Chart and pictures courtesy of Dupont Electronic Materials

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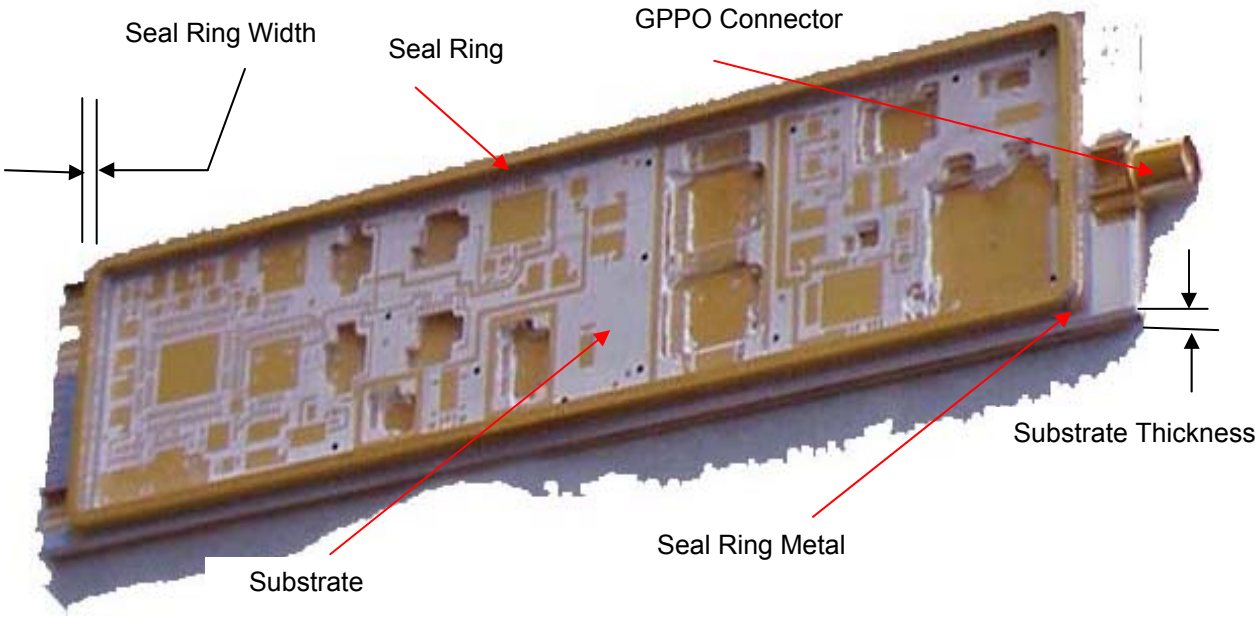
LTCC DESIGN GUIDELINES

SOLDERING DESIGN CONSIDERATIONS

Soldering of gold plated Kovar leads, pins, ring frames is standard practice in LTCC technology. Backside strength members or heat spreaders is also available. Heat spreaders are available in Al-Si-C Cu-Mo-Cu, Cu-W, Molybdenum, Ni-Fe alloys and Kovar depending on the specific LTCC ceramic



- Substrate overall thickness should be 40 mils minimum.
- Metal seal ring cross section should be 30 mils minimum. Ring frame corners should be radiused.
- Kovar leads and rings should be fully annealed prior to plating.
- Metal lead cross section and width should be minimized to reduce stress at the attachment site.
- Metal seal rings and leads should be plated with Ni and then Au.
- Metal seal ring aspect ratio height / width should not exceed 2.
- Preparatory metallization width should be, as a minimum, 2x wider than the seal ring, 2.5x is preferred. Top barrier metal should overlap bottom adhesion metal 5 mils / side. Metallization corners should be radiused to prevent solder pooling and reduce stress risers.
- Provide for dielectric solder dam material around solder sites. Dielectric should overlap barrier metal 2-5 mils/side.
- Lead or pin attachment sites should be 2x the width / diameter of the lead/pin.
- Circuitry passing under the seal ring should do so at least 2-3 tape layers below the ring (8-11 mils).

Please see our LTCC design CD for more in depth design information.

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LTCC DESIGN GUIDELINES

SOLDERING – THERMAL MATCHING

AVAILABLE SOLDER ALLOYS FOR LTCC

SOLDER ALLOY	REFLOW TEMPERATURE ºC
80 Au/ 20 Sn *	280ºC+
88 Pb / 10 Sn / 2 Ag *	267-299ºC
96 Sn / 4 Ag	221ºC
62 Sn / 36 Pb /2 Ag or 63 Sn / 37 Pb *	179ºC

*** Sea Ceramics Standard Solders**

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Sea Ceramic Technologies

THERMAL PROPERTIES OF CERAMICS AND METAL / METAL COMPOSITES

MATERIAL	Thermal Conductivity (W / M-°K @ 25°C)	Thermal Expansion (x10^{-6} / °C)	Density (gm / cc)
Aluminum	218	23	2.7
Cu	398	17.8	8.9
Mo	138	5.0	10.2
Ag	429	19	10.5
Au	318	14.2	18.9
Brush Wellman E20 (20% BeO / 80% Be)	210	8.7	2.06
Brush Wellman E40 (40% BeO / 60% Be)	220	7.5	2.30
Brush Wellman E60 (60% BeO / 40% Be)	230	6.1	2.52
Mo/Cu			
60/40	215	10.2	9.68
65/35	205	9.4	9.74
75/25	185	8	9.87
80/20	175	7.5	9.9
85/15	165	6.7-7	10.1
W/Cu			
90/10	170	6.5	16.9
87/13	175	6.9	16.4
85/15	180	7.2	16.1
82/18	185	7.8	15.5
80/20	185	8.3	15.2
Si-Al			
27/73	177	17.7	2.4-2.7
42/58	160	14	"
50/50	149	13	"
60/40	129	10.5	"
70/30	120	8.5	"
Si-C	272	3.7	3.21
Si	151	4.2	2.33
GaAs	54	6.5	5.26
Al-Si-C	>180	6.9 - 8	3.0
Cu-Mo-Cu			
5/90/5	151	5.1	
13/74/13	170	5.8	9.86
20/60/20	194	6.5	
25/50/25	213	7.3	9.55
33/34/33	251	8.6	9.34
Kovar	17	5.1-5.9	8.4
Alloy 45		7-7.5	8.3
Alloy 46	16	7.5	8.7
Epoxy-Glass	.16-.26	11-20	2.1
Dupont 951 LTCC	2.3	5.5	3.1
Ferro A6M/A6S	2	7.5	2.5
Heraeus CT2000 LTCC	2-3	8.5	3.05
99.5% BeO	250	7.5	2.85
AlN	167-223	4.5	3.21
96% Alumina	17-24	6.7	3.9
99.5% Alumina	37	6.7	3.9

***≥ 20 - 30 W/M°K with thermal vias**

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LTCC DESIGN GUIDELINES

ELECTRICAL AND MECHANICAL PROPERTIES OF LTCC

PROPERTY	DUPONT 943	DUPONT 951	FERRO A6M	FERRO A6S	HERAEUS HeraLock	HERAEUS CT 2000
Color	Light Blue	Blue	White	White	White	White
Available Fired Thickness (Mils)	1.8, 4.4, 8.8	1.7, 3.7, 5.2, 8.2	3.7, 7.4	3.7, 7.4	3.3	1.7 & 3.4
Dielectric Constant (K)	7.4	7.28	5.9	5.96	7.3	9.1
Loss Tangent	.2%	<.60%	.12%	.2%	-	<.26%
Mwave Insertion Loss (Db/in) @ 10Ghz	-	<.6	.18	-	-	-
Insulation Resistance	$>10^{12}$ Ohms	$>10^{12}$ Ohms	$>10^{12}$ Ohms	$>10^{12}$ Ohms	$>10^{12}$ Ohms	$>10^{12}$ Ohms
Breakdown Voltage	>1000 V/Mil	>1000 V/Mil	>900 V/Mil	>1000 V/Mil	>900 V/Mil	>1000 V/Mil
Flexural Strength	230 Mpa	207 Mpa*	>124 Mpa*	>124 Mpa*	-	310 MPa
Youngs Modulus (fired)	103 GPa	103 GPa	82 GPa	82 GPa	-	-
Temp. Coefficient of Freq. (T_f)	-	-	-	-	< 80 ppm	± 10 ppm
Fired Density	3.2	3.1 gm/cc	2.5 gm/cc	2.5 gm/cc	2.84	3.05
Surface Roughness	.64 µ m	<10 µ in	<15 µ in	<15 µ in	<.7 µ m	<1 µ in
Camber **	2 mils/in/in min.	2 mils/in/in min.	2 mils/in/in min.	2 mils/in/in min.	2 mils/in/in min.	2 mils/in/in min.
Shrinkage (Approximate)						
X,Y	19.5%±. .3%	12.7%±. 2%	14.8%±. 2%	14.5%±. 2%	.18%±. .013%	11.5%±. 2%
Z	10.3%±. .5%	15%±. 5%	25%±. 5%	35%±. 5%	36%	14%±. 5%
Metallizations	Au/Ag - Ag – Au & Cu	Au/Ag - Ag – Au & Cu	Au- Cu	Au/Ag - Ag – Au & Cu	Ag-Ag/Pt	Ag
Surface and Buried Resistor systems	Available	Available	Available	Available	Partial (See supplier)	Partial (See supplier)

* 3 point MOR test - 850°C firing temperature
** Minimum allowable camber

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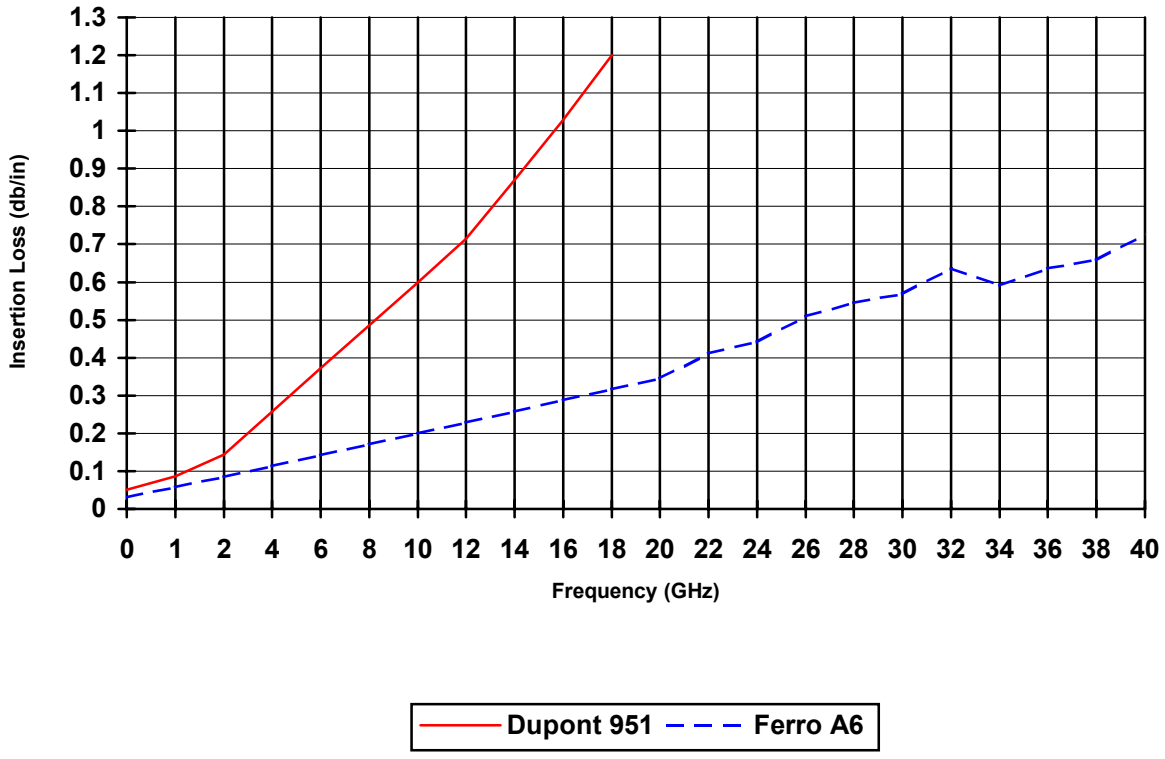
LTCC DESIGN GUIDELINES

MICROWAVE INSERTION LOSS OF FERRO A6 AND DUPONT 951 LTCC'S



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LTCC DESIGN GUIDELINES

DATA BASE AND DOCUMENTATION CONVENTIONS FOR LTCC DESIGNS

DOCUMENTATION PACKAGE

Please provide Sea Ceramics the following design documentation package prior to fabrication:

1. Gerber artwork database in 1-up format.
   - Design size should be 1:1
   - Aperture list (if not supplied in gerber 274X format)
   - Readme type text file with all pertinent design information (no. of layers, metals via sizes, etc.)
2. Artwork layer plots
3. Substrate top level drawing with dimensions and side view showing the layering scheme.
4. Product specification
5. Electrical net list

Design/Artwork packages may be sent to SEA CERAMICS at:

17755 Sky Park East, Suite CD
Irvine, CA 92614
Attn: Steve Scrantom

Please send data in zip format (Please do not supply data using self extracting .exe formats).

Drawing templates and this design guide are available for down loading upon request.

For those wishing to use the Internet for communication, **Sea Ceramics general e-mail address is:** **seaceramics@worldnet.att.net**

Those wishing **to obtain an electronic version** of this design guide may do so from Sea Ceramics Internet Home Page, or more in depth information is available on our LTCC design CD. **Our Internet address is http://www.seaceramics.com**

LTCC DESIGN GUIDELINES

ELECTRONIC DESIGN CRITERIA

Preferred Design Format
Sea ceramics preferred method of receiving data for artwork generation is in Gerber format. This is also the least costly because it eliminates conversion. DXF formats may be submitted for layout at additional cost. An additional week of lead time should be planned in the schedule if DXF formats are used. Please contact our marketing department for design charges and lead times.

Basic LTCC Layout Considerations
All designs should be submitted in one up configuration! Sea Ceramics will step and repeat all designs to best fit internal processing requirements.

All designs should include a **substrate outline** with all design layers using a **common origin**. This convention holds true for Gerber and AutoCad designs.

All design layers should be identified as to use and position in the stackup (See LTCC layering conventions diagram page 33).

All vias should be filled as flashes.

Cavity areas should be shown on its associated via layer as an outline. Please use a 5 mil decode for this structure with the outer most edge of the decode defining the cavity boundary. Please do not use overlapping polygons, use a single boundary.

All conductors should be rastor filled using Gerber type 274 X whenever possible.

Please do not include dielectric layers as part of a LTCC design. Substrate outline, vias, cavity outlines and conductors are the only required design layers.

Required Design Information
Please include an aperture list and a MS Note Pad based readme.txt file to facilitate loading of the design file into our CAD system. Required information in aperture list or readme file is:

a. Format - Gerber RS274, 274x, Fire 9xxx etc.
b. Zero suppression - Leading, trailing or none.
c. Type - Absolute or incremental
d. Digits - Integer/Decimal - 2/4, 2/5 etc.
e. Units - English or Metric.
f. Decode number, type and size (do not use decodes of zero). Please identify and describe any **custom decodes** clearly.
g. Part drawing or sketch defining all required dimensions and specifications. Please specify materials to be used in part fabrication.

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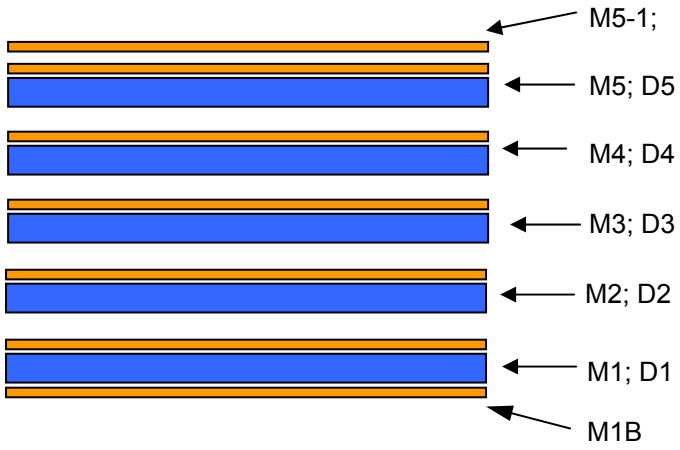
LTCC DESIGN GUIDELINES

LAYER CONVENTION FOR LTCC DESIGNS
SAMPLE 5 LAYER SUBSTRATE

CAD DESIGN LAYER CONVENTION FOR LTCC
(Sample part; for reference only)

TOP OF PART



Tape Layer	Tape Thickness	Via Designation	Via Diameters	Cond Designation	Description
1 Back				M1B	Ground
1 Front	3.7 mil	D1	8 mil	M1	Signal
2	5.5 mil	D2	6 mil	M2	VDD
3	5.5 mil	D3	6&8 mil	M3	VCC
4	8.3 mil	D4	10 mil	M4	RF
5	3.7 mil	D5	8 mil	M5	Ground

Multiple conductors on the same layer should be identified with a suffix -1, -2, -3... etc.

For example:
The second conductor on tape layer 5 would be identified as M5-1. A resistor would be identified as R5.
The second conductor on tape layer 7 would be M7-2.
Cavities should reside on via layers as outlines and be identified by layer. Please show cavities in the substrate cross section stackup.

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